REMARKS

The following remarks are made in response to the Office Action mailed February 24, 2005. Claims 1-35 were rejected. Claims 1-35 remain pending in the application and are presented for reconsideration and allowance.

Claim Rejections under 35 U.S.C. § 102

The Examiner rejected claims 1-35 under 35 U.S.C. § 102(b) as being anticipated by Ooishi, U.S. Patent No. 6,134,179 ("Ooishi"). The Examiner rejected independent claims 13, 18, 23, 29, and 33 based on the reasons stated for the rejection of claim 1. Applicants submit that Ooishi fails to teach or suggest the invention of independent claims 1, 13, 18, 23, 29, and 33.

Independent claim 1 recites a random access memory including a first line configured to receive first data signals between the first portion of memory cells and the data pads, and a second line configured to receive second data signals between the second portion of memory cells and the data pads, wherein the first portion of memory cells is configured to be made inaccessible to eliminate the first data signals and a first number of the data pads and a second portion of memory cells is configured to be made inaccessible to eliminate the second data signals and a second number of data pads. Independent claims 13, 18, 23, 29, and 33 include similar limitations as claim 1.

Independent claim 13 recites a random access memory including wherein the selected columns of memory cells communicate with data pads and the array of memory cells is configured to be reduced to eliminate a number of the selected columns of memory cells that communicate with the data pads. Independent claim 18 recites a random access memory including means for communicating the data signals between the banks and the data pads, and means for reducing the data pads and the addressable memory cells. Independent claim 23 recites a method for reducing storage capacity in a random access memory including preventing access to portions of the random access memory, and eliminating data pads electrically coupled to the portions of the random access memory where access is prevented.

Independent claim 29 recites a random access memory including wherein the first portion of data pads is electrically coupled to the first portion of memory cells through the first

portion of bit lines and the second portion of data pads is electrically coupled to the second portion of memory cells through the second portion of bit lines, the first portion of memory cells is configured to be made inaccessible by decoupling the first portion of data pads from the first portion of memory cells, and the second portion of memory cells is configured to be made inaccessible by decoupling the second portion of data pads from the second portion of memory cells. Independent claim 33 recites a dynamic random access memory including a first line configured to receive first data signals between the first portion of memory cells and the data pads, and a second line configured to receive second data signals between the second portion of memory cells and the data pads, wherein the first portion of memory cells is configured to be made inaccessible to eliminate the first data signals and a first number of the data pads and the second portion of memory cells is configured to be made inaccessible to eliminate the second data signals and a second number of the data pads.

Ooishi discloses a system to prevent the time necessary for complicated address processing, especially the redundancy determination for repairing defects or the process of internal address conversion, from limiting data transmission, and to improve operation performance of a semiconductor memory device. (Col. 1, lines 48-53). Ooishi also discloses increasing the speed of redundancy determination for a plurality of addresses while suppressing an increase in chip area and reducing power consumption at the time of self refresh. (Col. 1, lines 54-59).

Ooishi does not teach or suggest the invention of independent claim 1. Ooishi fails to teach or suggest **the first portion of memory cells is configured to be made inaccessible to eliminate the first data signals and a first number of the data pads and a second portion of memory cells is configured to be made inaccessible to eliminate the second data signals and a second number of data pads.**

Regarding claim 1, the Examiner submits that Ooishi discloses a random access memory in Figure 13 comprising a plurality of data pads, which are taught by data buses 626 and 628. (Office Action, page 2). Data buses 626 and 628 in Figure 13 do not teach or suggest the data pads recited in claim 1. The Examiner also submits that Figure 13 and the description for Figure 13 disclose that the odd portion of memory cells is configured to be made inaccessible (not

select) to eliminate the odd data signals and a first number of data bus 626, and the even portion of memory cells is configured to be made inaccessible to eliminate the even data signals and the second number of data bus 628. (Office Action, page 3).

Figure 13 shows a repeater used in a data system at the time of reading of the 1G bit semiconductor memory device. Referring to Fig. 13, the data from an odd-numbered address of data amplifier 624 from the array is transmitted through data bus 626 to a repeater 622, while the data from an even-numbered address is transmitted through data bus 628 to the repeater 622. Repeater 622 is controlled by a control circuit 630. The data transmitted by the repeater is applied to a multiplexer 632, and the data selected by multiplexer 632 is temporarily held by a latch 634. The two latched data are selected by multiplexer 636 and output through an output buffer 638 and a data terminal 640. (Col. 14, lines 15-28). Ooishi discloses data input/output terminals DQ0 to DQ31 in Figure 1 (Col. 6, lines 63-66) and DQ pads 608 for data input/output in Figure 14 (Col. 14, lines 33-35). Data buses 626 and 628 in Figure 13 are not data pads like DQ0 to DQ31 and DQ pads 608. Further, Ooishi does not disclose eliminating a number of the data pads DQ0 to DQ31 or DQ pads 608. In addition, even if data buses 626 and 628 did teach or suggest data pads, Oishi does not disclose the memory cells are configured to be made inaccessible to eliminate the data signals and a number of the data bus.

In view of the above, Applicants submit that the above rejection of claim 1 under 35 U.S.C. § 102(b) should be withdrawn. Likewise, the similar limitations of independent claims 13, 18, 23, 29, and 33 are also not taught or suggested by Ooishi for the same reasons as discussed above with reference to claim 1. Applicants submit that the above rejections of claims 13, 18, 23, 29, and 33 under 35 U.S.C. § 102(b) should be withdrawn.

Claims 2-12 further define patentably distinct independent claim 1. Claims 14-17 further define patentably distinct independent claim 13. Claims 19-22 further define patentably distinct independent claim 18. Claims 24-28 further define patentably distinct independent claim 23. Claims 30-32 further define patentably distinct independent claim 29. Claims 34-35 further define patentably distinct independent claim 33. Accordingly, dependent claims 2-12, 14-17, 19-22, 24-28, 30-32, and 34-35 are believed to be allowable over the cited reference. Allowance of claims 1-35 is respectfully requested.

CONCLUSION

In view of the above, Applicants respectfully submit that pending claims 1-35 are in form for allowance and are not taught or suggested by the cited references. Therefore, reconsideration and withdrawal of the rejections and allowance of claims 1-35 is respectfully requested.

No fees are required under 37 C.F.R. 1.16(b)(c). However, if such fees are required, the Patent Office is hereby authorized to charge Deposit Account No. 50-0471.

The Examiner is invited to contact the Applicant's representative at the below-listed telephone numbers to facilitate prosecution of this application.

Respectfully submitted,

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CERTIFICATE UNDER 37 C.F.R. 1.8: The undersigned hereby certifies that this paper or papers, as described herein, are being deposited in the United States Postal Service, as first class mail, in an envelope address to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 6 day of May, 2005.

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